

Vishay High Power Products

FlipKY®, 1 A Chip Scale Package Schottky Barrier Rectifier



FlipKY[®]

PRODUCT SUMMARY		
I _{F(AV)}	1 A	
V_{R}	40 V	

FEATURES

- Ultra low V_F per footprint area
- · Low leakage
- · Low thermal resistance
- · One-fifth footprint of SMA
- Super low profile (0.6 mm)
- · Available tested on tape and reel

APPLICATIONS

- · Reverse polarity protection
- · Current steering
- · Freewheeling
- Flyback
- Oring

DESCRIPTION

Vishay's FlipKY® product family utilizes wafer level chip scale packaging to deliver Schottky diodes with the lowest $V_{\textrm{F}}$ to PCB footprint area in industry. The four bump 1.5 x 1.5 mm devices can deliver up to 1 A and occupy only 2.3 $\,$ mm² of board space. The anode and cathode connections are made through solder bump pads on one side of the silicon enabling designers to strategically place the diodes on the PCB. This design not only minimizes board space but also reduces thermal resistance and inductance, which can improve overall circuit efficiency.

Typical applications include hand-held, portable equipment such as cell phones, MP3 players, bluetooth, GPS, PDAs, and portable hard disk drives where space savings and performance are crucial.

MAJOR RATINGS AND CHARACTERISTICS				
SYMBOL	CHARACTERISTICS	MAX.	UNITS	
V _{RRM}		40	V	
I _{F(AV)}	Rectangular waveform	1	٨	
I _{FSM}		250	A	
V _F	1 Apk, T _J = 125 °C	0.38	V	
T _J		- 55 to 150	°C	

VOLTAGE RATINGS				
PARAMETER	SYMBOL	FCSP140LTR	UNITS	
Maximum DC reverse voltage	V_{R}	40	V	
Maximum working peak reverse voltage	V_{RWM}	40	V	

FCSP140LTR

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ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average forward current	I _{F(AV)} 50 % duty cycle at T _{PCB} = 112 °C, rectangular waveform		1.0		
Maximum peak one cycle	l	5 μs sine or 3 μs rect. pulse	Following any rated load condition and with rated V _{RRM} applied	250	Α
non-repetitive surge current at 25 °C	IFSM	10 ms sine or 6 ms rect. pulse		21	
Non-repetitive avalanche energy	E _{AS}	$T_J = 25 ^{\circ}\text{C}, I_{AS} = 2.0 \text{A}, L = 5.0 \text{mH}$		10	mJ
Repetitive avalanche current	I _{AR}	Current decaying linearly to zero in 1 μ s Frequency limited by T_J maximum $V_A = 1.5 \text{ x } V_R$ typical		2.0	Α

ELECTRICAL SPECIFICATIONS (T _J = 25 °C unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS		TYP.	MAX.	UNITS
Maximum forward voltage drop		1 A	T _{.1} = 25 °C	0.43	0.48	V
	V _{FM} ⁽¹⁾	2 A	1J=25 C	0.51	0.56	
See fig. 1	V FM (1)	1 A	T _{.1} = 125 °C	0.34	0.38	
		2 A	1J = 125 C	0.46	0.53	
		$T_J = 25$ °C I_{RM} ⁽¹⁾ $T_J = 125$ °C	V _R = Rated V _R	10	80	μA mA
			V _R = 20 V	3.5	20	
			V _R = 10 V	2	10	
Maximum reverse leakage current	(1)		V _R = 5 V	1.5	5	
See fig. 2	IRM (')		V _R = Rated V _R	9	20	
			V _R = 20 V	3.5	8	
			V _R = 10 V	2.5	6	
			V _R = 5 V	2	5	
Maximum junction capacitance	C _T	V _R = 5 V _{DC} (test signal range 100 kHz to 1 MHz) 25 °C		-	160	pF
Maximum voltage rate of charge	dV/dt	Rated V _R - 10 000		V/µs		

 $^{^{(1)}\,}$ Pulse width < 300 $\mu s,$ duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	T _J ⁽¹⁾ , T _{Stg}		- 55 to 150	°C
Typical thermal resistance, junction to PCB	R _{thJL} (2)	DC operation	40	°C/W
Maximum thermal resistance, junction to ambient	R _{thJA}		62	C/VV

Notes

 $\frac{\text{dP}_{tot}}{\text{dT}_J} < \frac{1}{R_{thJA}} \quad \text{thermal runaway condition for a diode on its own heatsink}$

(2) Mounted 1" square PCB

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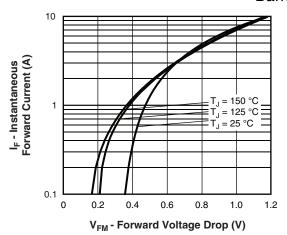


Fig. 1 - Maximum Forward Voltage Drop Characteristics (Per Leg)

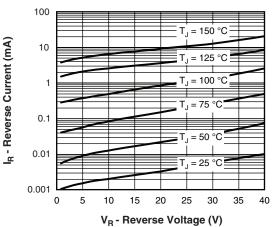


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage (Per Leg)

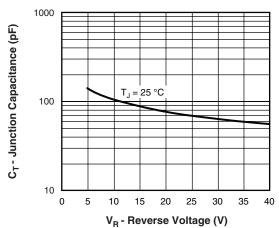


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage (Per Leg)

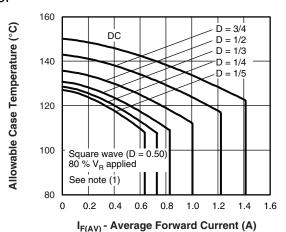


Fig. 4 - Maximum Allowable Case Temperature vs. Average Forward Current (Per Leg)

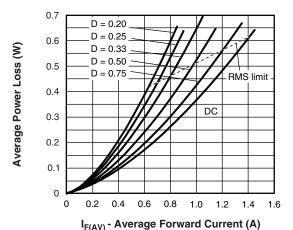
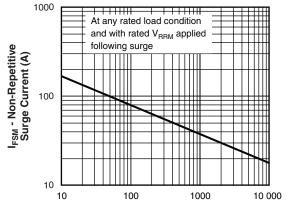


Fig. 5 - Forward Power Loss Characteristics (Per Leg)



 $t_{\rm p}$ - Square Wave Pulse Duration (μ s)

Fig. 6 - Maximum Non-Repetitive Surge Current (Per Leg)

Note

(1) Formula used: $T_C = T_J - (Pd + Pd_{REV}) \times R_{th,JC}$; $Pd = Forward power loss = I_{F(AV)} \times V_{FM}$ at $(I_{F(AV)}/D)$ (see fig. 6); $Pd_{REV} = Inverse$ power loss = $V_{R1} \times I_{R}$ (1 - D); I_{R} at 80 % V_{R} applied

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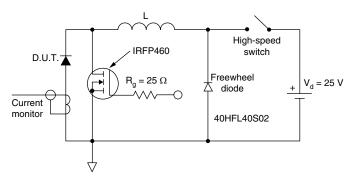


Fig. 7 - Unclamped Inductive Test Circuit

LINKS TO RELATED DOCUMENTS			
Dimensions http://www.vishay.com/doc?95282			
Part marking information	http://www.vishay.com/doc?95281		
Packaging information	http://www.vishay.com/doc?95062		



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